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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,145	03/30/2004	Srinivasan T. Rajappa	42P9347C	5430

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,145	RAJAPPA ET AL.	
	Examin r	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are presented for examination.

Information Disclosure Statement

2. The information disclosure statement filed on 05/10/2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because (i) references are listed in PTO-892 form instead of PTO-1449, and (ii) it is submitted under the wrong application number. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 15 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recite limitations "the first gate" and "the third second gate" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 17 recites the limitation "the first gate" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

4. Claim 15 is objected to because of the following informalities:

The following phrase is unclear in line 2 of claim 15:

"the first gate is a data flip-flop and the third second gate is a data flip-flop."

Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No.

6,748,513. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-28 of current application are unpatentable over claims 1-8, 1, 1, 9-10, 9, 9, 11-16 and 16-23 of U.S. Patent No. 6,748,513, respectively.

Claims 1-8, 1, 1, 9-10, 9, 9, 11-16 and 16-23 of US Patent no. 6,748,513 contain(s) every element of claims 1-28, respectively, of the instant application and as such anticipate(s) claims 1-28 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 11, 13, 18 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller et al. (USPN: 6,061,293), hereinafter, Miller

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claims 1 and 11, Miller teaches that the enable signal gets generated in response to the digital address strobe signal and digital address select signal, and the address packet provided once it appears on the address pin (e.g. see Col. 3, lines 9-67; Col. 4, lines 1-27 and Fig. 2). In the Miller's circuit shown in the Figure 2, the transparent latch 56 acts as flow-through circuit as described in this application and pulsed-transparent latches 62, 64 and 65 acts as flow-through gates as described in this application. This transparent latch takes the digital address strobe 36 and the enable signal 76 (called digital address select signal in this application) as inputs and produces the output signal (called enable signal in this application). This output (enable) signal further feed as enable signal and address 34 (called address packet in this application) as the data signal of the pulsed-transparent latches 60, 62, and 64. The address passes

thru these latches once it appears on the address pin as claimed in this application. In doing so, the synchronous interface of the address receiver circuit minimizes the address bus setup and hold time windows. Thus, the first component of the address packet can be provided to the chipset once the address packet appears on the address pin.

With respect to claims 13, 18 and 26, Miller teaches the claimed invention as described above. It is well known in the art that the A/D converter uses the differential amplifier to convert the analog signal/data into digital signal/data by comparing the input analog signal/data with the given reference voltage and producing the digital signal/data as an output. The Examiner herein taking Official Notice on this subject matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller.

As per claim 20, the memory controller with the interconnection of the chipset, the memory, the processor and the address receiver/decoder as claimed is well known in the art, however, it would not be commonly known to one of ordinary skilled in the art at the time of the current invention was made that how the address receiver decodes the address packet delivered from the processor. Miller, on the other hand, teaches

that the enable signal gets generated in response to the digital address strobe signal and digital address select signal, and the address packet provided once it appears on the address pin (e.g. see Col. 3, lines 9-67; Col. 4, lines 1-27 and Fig. 2). In the Miller's circuit shown in the Figure 2, the transparent latch 56 acts as flow-through circuit as described in this application and pulsed-transparent latches 62, 64 and 65 acts as flow-through gates as described in this application. This transparent latch takes the digital address strobe 36 and the enable signal 76 (called digital address select signal in this application) as inputs and produces the output signal (called enable signal in this application). This output (enable) signal further feed as enable signal and address 34 (called address packet in this application) as the data signal of the pulsed-transparent latches 60, 62, and 64. The address passes thru these latches once it appears on the address pin as claimed in this application. Accordingly, It would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the teachings of Miller in the commonly known memory controller. In doing so, the synchronous interface of the address receiver circuit minimizes the address bus setup and hold time windows. Thus, the first component of the address packet can be provided to the chipset once the address packet appears on the address pin.

8. Claims 19 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the "Background of the Invention" section of this application as applied to claims 1, 5, 6, 9, 13, 15 and 17 above, in view of Goldman et al. (USPN: 6,385,710), hereinafter Goldman.

As per claims 19 and 27, Miller teaches the address receiver as claimed in claims 1 and 11, however, this section does not teach that the flow-through gate is a latch. Goldman, on the other hand, teaches that a latch gets used as a flow-through gate (e.g. see lines 6-9 of abstract and lines 57-60 of column 1). Accordingly, It would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement or utilize latch as the flow-through gate (or transparent gate) as taught by Goldman for that of Miller. In doing so, first of all, the minimal propagation delay within the flow-through gate would have been achieved when latch is utilized as being compared to flip-flop or register circuits; second by reducing the system delay, it would avoid inefficient utilization of system bus bandwidth; increasing CPU and system throughput, therefore being advantageous.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100